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| EXAMINER | |
|---|---|
| LEE, HSIEN MING | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/046,893 | NAKAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Hsien-Ming Lee | 2823 | |

*-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-51* is/are allowed.

6)☒ Claim(s) *1,4,6-20,23 and 25-34* is/are rejected.

7)☒ Claim(s) *2-5,21-24 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claims 4, 23 and 40 are objected to because of the following informalities: the limitation "the impurity element" in claim 4, at line 24, claim 23, at line 7 and claim 40, at line 7, lacks antecedent basis. Changing into – *an* impurity element *in the impurity region* – is suggested. Appropriate correction is required.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 4, 6-20, 23 and 25-34 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12, 14, 16 and 17 of U.S. Patent No. 6,204,101 (Yamazaki et al.) in view of Ueda et al. (US 6,337,259) and Yamazaki et al. (US 6,077,731).

Claim 1, 6, 11 and 17, Yamazaki et al. (US '101) teach a method of manufacturing a semiconductor device, comprising steps of:

* adding a metal element to a semiconductor film having an amorphous

structure, i.e. adding the metal element by comprising the metal element in an amorphous semiconductor film (claim 14);

* crystallizing the semiconductor film having an amorphous structure to form a semiconductor film having a crystalline structure, i.e. crystallizing the amorphous semiconductor film to form a crystallized semiconductor film by heating (claim 17);

* selectively adding a rare gas element to the semiconductor film having a crystalline structure to form an impurity region, i.e. adding the rare gas (i.e. Ar, He and Ne) to the crystallized semiconductor film by heating the crystallized semiconductor film in an atmosphere comprising at least a material selected from the group consisting of Ar, He and Ne to form the impurity region (i.e. a desired region in the crystallized semiconductor film that is doped with the rare gas by heating the crystallized semiconductor film in the rare gas atmosphere) (claim 12); and

* gettering the metal element to the impurity region to selectively remove or reduce the metal element in the semiconductor film having a crystalline structure, i.e. gettering by reducing the metal element in the crystallized semiconductor film by heating (claim 16).

Yamazaki et al. (US '101) do not claim the step of removing the impurity region.

However, the removing step is a necessary step prior to proceeding subsequent processing to complete the formation of the semiconductor device, as evidenced by Ueda et al. Ueda et al. in an analogous art teach steps of: (1) adding a metal element (i.e. Fe,Co, Ni, Cu, Ru, Rh, Pd, Os, Ir, Pt or Au) to an amorphous silicon film 22 by spin coating a nickel-containing film 23 thereon (claim 2 and Fig.1B); (2) crystallizing the amorphous silicon film 22 to form a crystalline silicon film 24 by heating (claim 1); (3) doping impurity into the crystalline silicon

film to form an impurity region 27 by a first gettering step (claim3 and Fig.1E) ; (4) gettering the metal element to the impurity region 28 (derived from region 27) to selectively remove or reduce the metal element in the crystalline semiconductor film 24 in second gettering step (claim 1and Fig.1F); and (5) removing the impurity region 28 (Claim 4 and Fig.1G).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to remove the impurity region as taught by Ueda et al. after the gettering step of Yamazaki et al. (US '101), since by doing so it would prevent the metal element from diffusing into the remaining crystalline semiconductor film (i.e. a gettered region, col.14, lines 5-13, Ueda et al.), which would is beneficial to the formation of the semiconductor device as shown in Fig. 1L of Ueda et al.

In re claims 16 and 33, Yamazaki et al. (US '101) claim that the metal element is for the purpose of promoting crystallization of the amorphous semiconductor film but do not claim that that the metal element is one kind or plurality of kinds of element selected from the group consisting of Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

However, Ueda et al. expressly teach that Fe,Co, Ni, Cu, Ru, Rh, Pd, Os, Ir, Pt and Au are metal elements good for acceleration of the crystallization (claim 2).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the aforementioned metal elements as taught by Ueda et al. as the metal element of Yamazaki et al. (US '101), since by this manner it would promote the formation of the crystalline semiconductor film.

In re claims 4 and 23, Yamazaki et al. (US '101) in view of Ueda et al. teach all the limitations with exception of irradiating the semiconductor film with strong light or laser light

from a front surface or a reverse surface to activate impurity element after the removing the impurity region.

However, irradiating the semiconductor film by strong light or laser to activate the impurity element in the semiconductor film is a necessary step for forming source/drain region in the semiconductor device, as evidenced by Yamazaki et al. (US '731) (col. 43, lines 26-31).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the laser light irradiation as taught by Yamazaki et al. (US 7310) in the method of Yamazaki et al. (US '101) in view of Ueda et al., since by doing so it would satisfactory form impurity regions for source/drains.

In re claims 7, 9, 26 and 28, Yamazaki et al. (US '101) in view of Ueda et al. do not claim and teach that the crystallizing is conducted by irradiation of the semiconductor film having an amorphous structure with strong light; and the crystallizing is conducted by heat treatment and irradiation of the semiconductor film having an amorphous structure with strong light.

However, utilizing irradiation from strong light and heat treatment for crystallizing are well known practice in the art, as evidenced by Yamazaki et al. (US '731), wherein a strong light from a laser is performed for crystallization besides a heat treatment for obtaining high crystallinity (col.38, lines 48-59).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the strong light such as laser and heat treatment as taught by Yamazaki et al. (US '731) in the method of Yamazaki et al. (US '101) in view of Ueda et al., since by doing so it would achieve high crystallinity in the crystallized semiconductor film (col. 38, lines 56-60, Yamazaki et al. US '731).

In re claims 8, 10, 27 and 31, Yamazaki et al. (US '101) in view of Ueda et al and Yamazaki et al. (US '731) inherently teach that the strong light is emitted from a lamp selected from the group consisting of a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, and a high-pressure mercury lamp. In particular, Yamazaki et al. (US '731) teach utilizing an ultraviolet lamp or an infrared lamp for crystallization (col.39, lines 8-10), wherein the ultraviolet and infrared lamps inherently refer to a halogen arc lamp because the halogen arc lamp produces wide wavelength from infrared rays to ultraviolet rays.

In re claims 12-15, 30, 32, Yamazaki et al. (US '101) in view of Ueda et al. and Yamazaki et al. (US '731) also teach that the gettering is conducted by heat treatment ( col.78, lines 17-22, Yamazaki et al. US '731) and irradiation of the semiconductor film with strong light (col.78, lines 8-16,Yamazaki et al. US '731); and the strong light is emitted from ultraviolet or infrared rays, which inherently include the aforementioned halogen lamp (col. 79,lines 34-39, Yamazaki et al. US '731).

In re claims 18-20, 25, 29 and 34, Yamazaki et al. (US '101) teach a method of manufacturing a semiconductor device, comprising steps of:

* adding a metal element to a semiconductor film having an amorphous structure, i.e. adding the metal element by comprising the metal element in an amorphous semiconductor film (claim 14);

* crystallizing the semiconductor film having an amorphous structure to form a semiconductor film having a crystalline structure, i.e. crystallizing the amorphous semiconductor film to form a crystallized semiconductor film by heating (claim 17);

* selectively adding a rare gas element to the semiconductor film having a crystalline structure to form an impurity region, i.e. adding the rare gas (i.e. Ar, He and Ne) to the crystallized semiconductor film by heating the crystallized semiconductor film in an atmosphere comprising at least a material selected from the group consisting of Ar, He and Ne to form the impurity region (i.e. a desired region in the crystallized semiconductor film that is doped with the rare gas by heating the crystallized semiconductor film in the rare gas atmosphere) (claim 12); and

* gettering the metal element to the impurity region to selectively remove or reduce the metal element in the semiconductor film having a crystalline structure, i.e. gettering by reducing the metal element in the crystallized semiconductor film by heating (claim 16).

Yamazaki et al. (US '101) do not claim the steps of : (1) forming a first mask on the semiconductor film having a crystalline structure; (2) forming a second mask on the semiconductor film having a crystalline structure; and (3) selectively removing the semiconductor film; (4) that the impurity region and a part of the semiconductor film having a crystalline structure are removed in the selectively removing the semiconductor film; and (5) that the second mask is provided at a position on an inner side of the ends of the first mask.

However, the aforementioned three steps are necessary procedure for forming the semiconductor device, as evidenced by Ueda et al. Ueda et al. teach forming a first mask 16 on the crystalline semiconductor film 14 for the purpose of forming impurity region 17 (Fig.7D-7E); and forming a second mask (not shown) on the crystalline semiconductor film 14 for removing peripheral portion 19 of the semiconductor film 14 (Fig.7F and col. 2, lines 56-62); selectively removing the semiconductor film, i.e. selectively removing the peripheral portion 19 of the

semiconductor film 14; the impurity region 17 and a part of the semiconductor film 19 having a crystalline structure are removed in the selectively removing the semiconductor film 14 (Figs 7E-7F); and that the second mask (not shown ) is provided at a position on an inner side of the ends of the first mask 16, i.e. the second mask (not shown ) is smaller than the first mask 16.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the aforementioned steps as taught by Ueda et al. in the method of Yamazaki et al (US '101), since by this manner it would make an island-shape active region for TFT (col.14, lines 55-58).

***Allowable Subject Matter***

4. Claims 35-51 are allowed.

The prior art of record, Yamazaki et al. (US '101) claim the instant invention, as stated above, but no not claim forming a *first mask* on a semiconductor film having an *amorphous* structure for selectively adding the metal element ; forming a second mask on the semiconductor film having a crystalline structure; and selectively removing the semiconductor film.

Yamazaki et al. to US '731 also neither teach nor suggest forming a *first mask* on a semiconductor film having an *amorphous* structure for selectively adding the metal element. Instead, the way that the metal element is added into the semiconductor film in Yamazaki et al. (US '731) is not *selectively added* by forming the *first mask* but by spin-coating.

5. Claims 2, 3, 5, 21, 22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art (US '101) does not claim that one kind or a plurality of kinds of elements selected from the group consisting of *H, H2, O, O2, and P are added in addition to the rare gas* element (claims 2, 21); that the selectively adding a rare gas element is conducted in an atmosphere containing a *rare gas element and water vapor* (claims 3, 22); and oxidizing a surface of the semiconductor film having a crystalline structure with *a solution containing ozone after the crystallizing* (claims 5, 24).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohtani et al. to US 5,923,962 and Makita et al. to US 6,013,544 teach common subject matter as claimed.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

May 17, 2003